Day 1 - Tuesday (Nov 3)

Time	Main Stage / Room 1	Room 2	Room 3	Room 4	Room 5
8:30 8:45	Check In & Breakfast				
9:00 9:15 9:30 9:45 10:00	KN1 - Conference Opening : [R1 : 75 min] Fiona Treacy Joe Barry (VT Electron)				
10:15 10:30 10:45	Break (Demo Time Starts) EXTRA 15MINS OPENING DAY!				
11:00 11:15 11:30 11:45 12:00 12:15	SS1: Charting the next Frontier; ADI's Long Term Technology Strategy Santiago Iriarte, Paul Ferguson, Sam Zhang, Zoran Zvonar [90min]	A Novel Design Methodology for High-Current Power Trains Giacomo Petracca A 0.16mm2 4mW 95dB SNR in 450kHz bandwidth CTDSM in 40nm Roberto Maurino (Author - Praveen Varma) xVienna - Architecting the FreqGen for a Multi-Carrier Homodyne Detection Sensing System - with a TERRIBLE Reference Niall Kearney !!CLOSED SESSION!!	Evolution of Timing ECO Methodologies: From Iterative Closure to Intelligent Signoff Saumya Kumari Intelligent Design and Process Exploration Artur Sokolowski !!CLOSED SESSION!! DQA Dashboard: AI-Assisted Platform for VC SpyGlass CDC/RDC/LINT Analysis and Resolution Juancarlos Nunez	Agents in the Loop: Applying Specification-Driven Development to AI-Assisted Silicon Validation Juan Morant Ricardo Salvador AI-Assisted Analog-to-RTL Conversion for FPGA Prototyping of Mixed-Signal BMS ASICs Yeshvanth Muniraj Ricardo Salvador Centralized Motor Control for SDVs: Meeting OEM Demands for Safety and Flexibility Derek Burke & Eduardo Santos Navarro	Closed Loop – The Ultimate Goal of GMR Multiturn Sensor Development Niclas Teicher Towards Unlimited Turn Counting: Functional Closed-Loop GMR Sensor via Overpass Bridges Jochen Schmitt My NPN Did What? X-Ray Investigation Reveals All On Low Power Reference Radiation Sensitivities! Luke Guinane
12:30 12:45	LUNCH	Cumulus (AD5529R) How the Packaging Toolbox facilitated First Silicon Release in Two Very Different Packages Cillian Burke	MCM-Optimized Polyphase FIR Decimation for Precision ADCs Mauro GarciaFranco	LUNCH	LUNCH
13:00 13:15	LUNCH + ETC Extra				
13:30 13:45 14:00 14:15 14:30 14:45	SS2: Measurement AI and MMC: LB & HT Piotr Sloniec with Brian Sweeney [90min]	LUNCH How Close is Too Close: Benchmarking 16 nm MRAM NVM Under Magnetic Field Interference Ricky Anthony Integrated eSOA and Thermal Analysis for Intrinsic Reliability De-Risking of Large-Geometry EP20S DMOS John Meskell	AI-Assisted Cross-Domain Debug and Analysis for Physical Design Closure Christopher Veloso & Ivet Marie Lontajo Closing the Invisible Gap: Automated Shield Line Verification for Robust LVS Sign-Off Kimberly Garavillas	Lossless ECG Compression for Battery-Efficient Wearable Health Monitors Uraz Cakaci Local Linear Regression with Adaptive kNN Kernels for Sparse-Lead ECG Reconstruction Vicent Torres Adaptive ANC for the Next Generation Hearables Joris Hansen	LUNCH Virtual Prototyping as Strategic Enabler for ADI 3.0: Accelerating Time-to-Market for ADI and Its Customers Manali Mondal Left-Shifted Audio Firmware Validation Using a SystemC Virtual Platform Across Mead Subsystems Kajal Majalatti (Author - Amol Nikade)
15:00 15:15	Break (Demo Time Ends)				
15:30 15:45 16:00 16:15	Ray Stata Fireside chat				
16:30 16:45 17:00 17:15 17:30 17:45 18:00 18:15	Poster Expo + Patent Expo + Ext Researcher Expo [R1: 2 Hr]				
18:30 18:45 19:00 19:15	EMEA Connect - mix & mingle Pizza & Beer (Treehouse)				
19:30 19:45 20:00 20:15	ADI Ireland 50th @ The Fitzgerald Suite Evening Event				
20:30 20:45 21:00 21:15 21:30 21:45	Beer & Music ADI Music Open Mic @ The Treehouse				
22:00	Conference End Day 1 - Chat / Beer / Mingling can continue				

Day 2 - Wednesday (Nov 4)

Time	Main Stage / Room 1	Room 2	Room 3	Room 4	Room 5
8:30 8:45	Check In & Breakfast				
9:00 9:15 9:30 9:45 10:00	KN2 - From Silicon to Systems Jason Griffin [R1: 60mins]				
10:15 10:30 10:45	Break (Demo Time Starts)				
11:00 11:15 11:30 11:45 12:00 12:15	SS3: Humanoids - Technology, Intelligence and Real-World Challenges Dara O'Sullivan [90min]	Shift Left with Magnetic Sensing – Enabling Early Customer Evaluation of Complex Electromechanical Systems Adam Fahey Achieving Millidegree Accurate Magnetic Encoders Via Electrical Self-Alignment Colin Gill ATE readiness for Silicon test with VISTA Meghana Sripada	Stop Wasting Seeds-Smarter UVM Regressions Abhimanyu Singh Unleashing UVM-MS Paul Wright Catching the Critical Few: Smarter Floating-Node Verification Miguel Ruiz	Collaborating with NVIDIA on Data Center Power Stability using ADI Technology Michael Meehan !!CLOSED SESSION!! Granite Heterogeneous Compute State of the ART AI Audio processor Eoin English Sparkle: Redefining Low-Latency Wireless Systems Martina Balbi	Analyzing SoC Performance and Power Before RTL: A Multi-Fidelity Shift-Left Methodology Sravan Namala AI-Assisted Simulation Environment Migration Across EDA Vendors for Digital Ips Vishwas Deshpande PDK Framework for Monolithic GMR Multiturn Sensors Wayne Doyle
12:30 12:45	LUNCH	Beyond 20 GHz: Embedding a Wideband 22GHz & 33GHz RF Source into Final Test Emmanuel Abalain	Smart Regression Triage: Automated SVA Failure Analysis with Design Change Correlation Kirti Kansal	LUNCH	LUNCH
13:00 13:15	LUNCH + ETC Extra				
13:30 13:45 14:00 14:15 14:30 14:45	SS4: From AI-First Success To AI-Native Silicon Development - Syam Veluri, Nimay Shah !!CLOSED SESSION!! [90min]	LUNCH Humanoid Hand Learnings: Observation to Compensation Mark Donegan Enhancing Efficiency of Class-D Audio Amplifier Systems Through True Peak Estimation and Smart Release Rakhel Parida	A Dual Loop FVF-Based Architecture for Area-Efficient Sub Nanosecond Settling SAR DAC Reference Bijaya Adhikari An 11.5 nV/√Hz 0.12 mm2 Capacitive Programmable Gain Amplifier for Hall-Sensor AFE Mohamed Atef Hassan	Optimization of Neural Network inference using Xtensa compiler tool for HiFi DSPs Charles Fox State-Based PWM Configuration Tooling: Bridging System-Level Intent to Hardware Implementation David Oleary Enabling Eval Shift-Left with VISTA through DV: Bridging Eval and DV Paolo Crosetto	LUNCH Silicon Trust in a Quantum World Maitreyi Ashok MKA meets multidrop: Optimizing MACsec Key Agreement for Automotive 10BASE-T1S Guillermo Oliver
15:00 15:15	Break (Demo Time Ends)				
15:30 15:45 16:00 16:15	KN4 - Closing Plenary: [R1 : 60 min]: Fellows Session - The Winners will be the Thinkers				
16:30	Patent Milestone Awards - Jed Hurwitz [R1: 15 min]				
16:45	Innovation Awards Presentation - Javier Calpe [R1 : 15 min]				
17:00	Conf Awards Presentation - Fiona [R1 : 15 min]				
17:15	Conference Close - Fiona [R1 : ~5min]				
17:30	Conference End Day 2				